Introduction to Computer Systems CCE1011

January 2008

(In the exam you were asked to answer 4 questions in 2.5 hours

1. Write short notes on the following:

(i) an instruction fetch cycle;
(ii) processor databuses - internal and external
(iii) static and dynamic RAM
(iv) user virtual memory
(v) operating system software

(25 marks)

2. A computer uses cache memory together with the main memory. The computer uses 32- bit wide databus on a memory organised in a byte fashion.

The cache has 256, 32-bit memory cells, organised in four sets of 2 blocks per set.

The main memory has a total of 64Kbyte addresses.

(i) How many bits are needed for a main memory address? (2 marks)

(ii) How many bytes are there in a block that is transferred from main memory to cache? (3 marks)

(iii) Organise these bits in a TAG, SET, WORD fields for transfer between memory and cache. (6 marks)

(b) The cache is five times faster than main memory. For the organisation above a program consists of 500 bytes from location 0 to location 499 in main memory is to be executed. The program has a loop between address 128 and 255. This loop is repeated five times. Assuming a main memory access takes 100 ns, and negelecting execution time, calculate:

(i) the time the program takes to execute if it is run directly from main memory without a cache.

(ii) the time the program takes to execute run with a main memory and a cache memory as in (a) above.

(14 marks)

3. (a) Define the parameters that contribute to the access time when data is to be transferred between a magnetic disk and main memory. (5 marks)

(b) Distinguish between access of data on a magnetic disk and access using an optical disk. (5 marks)

(c) RAID Levels 3 and 4 use extra parity bits in writing the data to disc. Why are these parity bits used? (5 marks)

(d) A magnetic disk has a diameter of 10 cm. Tracks are manufactured on the platter starting at r = 2.5cm to r = 4.5 cm. Each track is spaced by .5 mm. The data is organised in 200 sectors per circumference, each sector containing 1024 bytes of data.

Calculate

(i) the number of tracks;

(ii) the maximum and minimum bit density along a track.

(iii) If the platter rotates at a speed of 240 revs per minute, calculate the average rotational delay.

(10 marks)

4 A 256 byte dynamic RAM is organised as eight 256 X 1 bit IC's. Each IC uses a row address column address design. The number of rows and columns is the same.

(a) Design the circuit showing clearly the input address bits, the row and column decoders, and the row and column bit lines, in detail, for at least one row and one column. (10 marks)

(b) For your design, given the input address pattern 01110010 indicate the bit cell chosen as $C_{i,j}$ where i is the row number, and j is the column number.

(6 marks)

(c) Given the design in (a) above as a basic building block. organise a 1K byte main memory made up of these building blocks.

Show clearly the number of the building blocks necessary and how the whole address range from address 0 to address 1023 is obtained. (9 marks)

5. (a) Slow speed peripherals can be accessed using three different types of techniques. Define the three types, and show clearly the advantages and disadvantages of each type. Mention the type which is the most efficient with respect to CPU time.

(10 marks)

(b) Main memory has system programs and user programs. Describe how these programs are executed and the precautions so that user programs do not interfere with each other. (5 marks)

(c) A user program can only be partially loaded in a main memory that is designed as a paged memory system.

(i) Why is this possible?

(ii) What are the overheads in CPU hardware necessary when such a system is used? (10 marks)

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