Introduction to Computer Systems CCE1011

January 2011
Answer ANY FOUR questions

1. Write short notes on the following:

(i) a stack pointer register;
(ii) asynchronous and synchronous data transfer
(iii) refresh circuit in a dynamic RAM
(iv) RAID levels 0 to 2 in HDD
(v) parity bits in a RAM

(25 marks)

2. (a) A computer uses cache memory together with the main memory. The computer uses 32- bit wide databus on a memory organised in a byte fashion. The cache has 128, 32-bit memory cells, organised in four sets of 2 blocks per set. The main memory has a total of 64Kbyte addresses.

(i) How many bits are needed for a main memory address? (2 marks)
(ii) How many bytes are there in a block that is transferred from main memory to cache? (3 marks)
(iii) Organise these bits in a TAG, SET, WORD fields for transfer between memory and cache. (6 marks)

(b) The cache is five times faster than main memory. For the organisation above a program consisting of 640 bytes is loaded into memory starting from location 1024 to location 1663 in main memory. The program has a loop between address 1152 and 1343. This loop is repeated five times. Assuming a main memory access takes 100 ns, and neglecting execution time, calculate:
(i) the time the program takes to execute if it is run directly from main memory without a cache.
(ii) the time the program takes to execute run with a main memory and a cache memory as in (a) above.

(14 marks)

3. (a) Define the parameters that contribute to the access time when data is to be transferred between a magnetic disk and main memory. (5 marks)
(b) Distinguish between access of data on a magnetic disk and access using an optical disk. (5 marks)
(c) A magnetic disk has a diameter of 10 cm. Tracks are manufactured on the platter starting at r = 2.5cm to r = 4.8 cm. Each track is spaced by .05 mm. The data is organised in 200 sectors per circumference, each sector containing 1024 bytes of data. Calculate
(i) the number of tracks; (3 marks)
(ii) the maximum and minimum bit density along a track. (3 marks)

(iii) If the platter rotates at a speed of 1240 revs per minute, calculate the average rotational delay. (4 marks)

(d) How is synchronization of the head to a sector achieved in the hard disk to ensure proper data transfer? (5 marks)

4 (a) A benchmark program is run on a 1GHz processor. The executed program consists of 100,000 instruction executions. The instructions have the mix and parameters given in Table 1.

Instruction Type	**Instruction Count**	**Clock cycles per Instruction**
Integer Arithmetic	38,000	1
Data Transfer	22,000	2
Floating Point Arithmetic	35,000	3
Control Transfer	5,000	4

Table 1

For this program calculate:

(i) the effective CPI, clocks per instruction (5 marks)
(ii) the MIPS rate (4 marks)
(iii) the execution time of the program in microseconds, (μs). (4 marks)

(b) (i) A 64 bit dynamic RAM is organised using RAS and CAS. Draw the diagram of the IC, showing clearly the rows and the columns of the IC. (7 marks)

(ii) Within the diagram draw the memory cell at position 101011. State any assumptions made (5 marks)

5. (a) Slow speed peripherals can be accessed using three different types of techniques. Define the three types, and show clearly the advantages and disadvantages of each type. Mention the type which is the most efficient with respect to CPU time. (8 marks)

(b) (i) Why is a Table Look Aside Buffer, (TLB), used in a processor? (6 marks)

(ii)Mention at least THREE parameters that are included within an entry of the TLB. In each case describe briefly the reason for the inclusion of the parameter. (6 marks)

(iii) Does a program need to be fully loaded contiguously in main memory when a paged memory system is used? Give reasons for your answer (5 marks)