CCE3013 Computer Architecture

Tutorial 1

1. A processor pipeline with four stages - Fetch,Decode,Execute,Writeback, has the following sequence of instructions:

```
        ADD   R0,R1,R2
        MUL   R3,R2,R4
        MOV   #05, R0
LAB1:   INC   R4
        DEC   R0
        JNZ   LAB1
```

Initially R0 =20, R1 = 10, R2=05, R3=25

(i) Using the pipeline show where there are:
Data dependencies and branch delays

(ii) Assuming each pipeline stage executes in one time unit, what is the overall speed up compared to direct sequential execution, taking into account any pipeline stall that is necessary for correct operation.

(iii) Suggest alterations in the instruction sequence that can improve the efficiency of the pipeline, and work out the new speedup factor.

2. For the program in question 1 above, and assuming initially R0 =20, R1 = 10, R2=05, R3=25; work out the contents of the buffer at the output of the execute stage (before writeback), at each clock. Ignore data dependency but assume the loop is rolled out.

3. (a)Describe three ways in which a conditional branch instruction can be handled in a pipeline.

(b) A processor has a four stage pipeline. The processor also uses an instruction cache and a data cache. The system clock operates at 500MHz, and each pipeline stage requires two clocks for proper operation. An external memory read/write requires 30ns. A programme has 10% of the instructions requiring external memory access. 20% of instructions require data operands, and 10% of these operands need to be accessed from main memory.

(i) Calculate the average number of clock cycles that are necessary to allow for the pipeline stalls, and the resultant speed up compared to sequential execution.

(ii) Additionally pipeline stalls due to data dependency increase the execution penalty by 0.5 clock cycles. To keep the resultant speed up factor the same as in (i) it is necessary to reduce the percentage of data operands that are required from main memory. Calculate this new percentage value.

4 A non-pipelined processor has a clock of 2 GHz and an average CPI (cycles per instruction) of 3.5. An upgrade to the processor introduces a six stage pipeline. However due to additional delays in the pipeline the clock is reduced to 1.5GHz.

(a) What is the throughput in MIPS for each processor?

(b) What is the speed up factor?