Computer Logic and Organisation CCE1012 June 2009

Answer ANY FOUR questions. All questions carry equal marks.

1.   Write short notes on the following:

     (i)   disk access time
     (ii)   program counter register and memory address register
     (iii)   synchronous and asynchronous memory access
     (iv)   checking for overflow in integer addition
     (v)   error correcting codes in RAM

                            (25 marks)

2.   (a) Why is a replacement algorithm necessary when operating cache memory?
                            (5 marks)

     (b) A 4Kbyte cache uses 4 sets of 2 blocks each in conjunction with a 1 Mbyte main memory.

          (i)   How many bits are needed for a main memory address?
                            (3 marks)

          (ii)   Organise these bits in a TAG, SET, WORD fields for transfer between memory and cache.   (5 marks)

     (c) A program resides in main memory from address 0 to address 5119. The program has a loop from address 1024 to address 3583, and the loop is repeated (executed) ten times. A main memory access takes 50 nanoseconds and the cache is five times faster than main memory. Assuming the Most Recently Used Replacement Algorithm is used in the cache, calculate
          (i) the time the program takes to execute in the system using main memory and cache.   (9 marks)
          (ii) the main memory blocks that reside in the cache at the end after program execution is finished

                            (3 marks)

3.   (a) Distinguish between access of data on a magnetic disk and access using an optical disk.   (5 marks)

     (b)In main memory, access is to an individual address level. What is the minimum (smallest) level that can be accessed from a hard disk? Give reasons for your answer.   (5 marks)

     (c) A magnetic 'hard disk volume' operates at a constant linear velocity when reading/writing to tracks on the surface. The radius of the innermost track is 5 cm

and that of the outermost track is 10 cm. The linear velocity the system uses is 400π cm per second.

Calculate the range (smallest and highest) angular velocity, in revolutions per minute, needed to maintain the constant linear velocity, given above, when accessing data from any track on the surface. (10 marks)

(d) What does RAID mean in conjunction with computer memory storage, and why is it used?

(5 marks)

4   (a) The traditional instruction fetch-execute cycle of a processor is no longer used in today's processors. Indicate using at least one example, how the instruction fetch-execute is organised in today's processors. (5 marks)

(b) Sketch a block diagram of a 2 to 4 decoder. Explain briefly how such a decoder can be used, in conjunction with a given size of RAM IC's, to design a bigger (more addresses) RAM. (8 marks)

(c) A digital combinational logic system is to be designed to give an output logic '1' whenever three or more out of four available inputs are at logic '1' simultaneously. Work out the truth table, and hence use Karnaugh map techniques to minimize the output logic function. (12 marks)

5.   (a) For an 8-bit two's complement representation, what is the valid range of integers? (2 marks)

(b) How is the subtraction operation obtained within an ALU using only a parallel full adder (5 marks)

(c) A floating point number representation uses 1 bit for the sign, 7 bits for the significand, and 6 bits for the exponent. The mantissa is normalized using the IEEE standard (as 1.xxxx where the leading one is not included in the significand), and the exponent uses two's complement excess code. Show how the following two numbers are represented:

(i)   21.25 (5 marks)
(ii)   – 0.02 (5 marks)

(d) Using Booth's algorithm develop the multiplication, with 11 as the multiplier and (-13) as the multiplicand, using 5-bit two's complement representation for the numbers. (8 marks)

Tutorial   Computer Arithmetic

1.   A logic system is to be used in a game. There are four participants. If two or more of them give the same answer a lamp lights, otherwise the light remains off.
Work out the required truth-table and hence use karnaugh map techniques to minimise the output logic function.

2.   Minimise using Karnaugh maps the following logic system, given in minterms.

$$F(A,B,C,D) \ = \ \Sigma \ (0, 1, 6, 7, 8, 9, 12, 13)$$

3.   Use two's complement arithmetic with a 6 bit representation. What is the representation for the following decimal integers.

      (i)   23   (ii)   -14   (iii) –1   (iv)   31

      What is the valid range for the 6-bit reprersentation?

4.   Multiply the following two integers in 5-bit two's complement representation using Booth's algorithm. Show clearly the working steps of the operation.
            Multiplicand 11   Multiplier – 6

5.   A floating point representation uses one sign bit, six bits for the mantissa and five bits for the exponent. The mantissa uses normalised representation and the exponent uses two's complement excess code. Give the representation for the following decimal numbers.
      (i) 11.2   (ii) - 3.25   (iii) 0.04