CPU register control

- Register controls on input and output

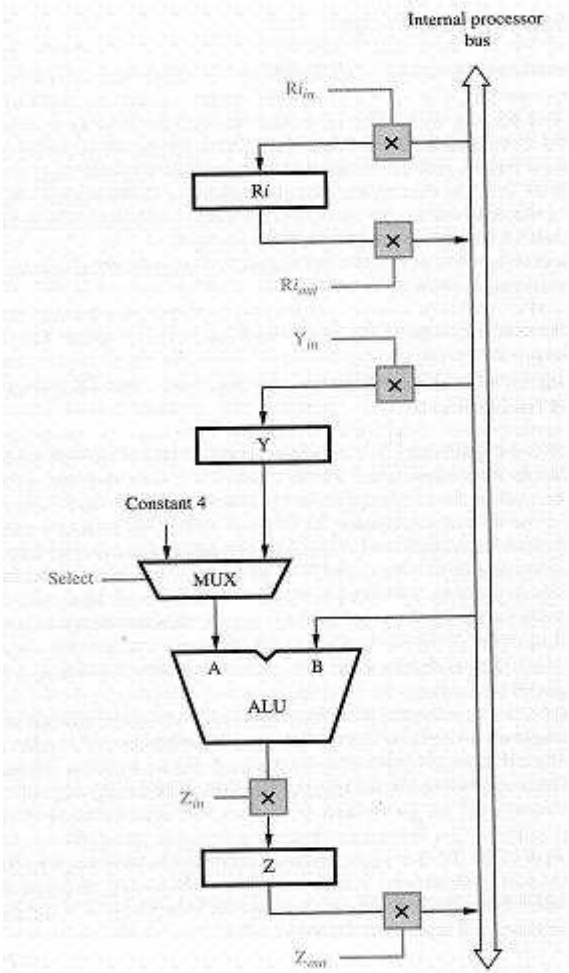

Figure 7.2 Input and output gating for the registers in Figure 7.1.

Internal data bus

- A Unibus structure

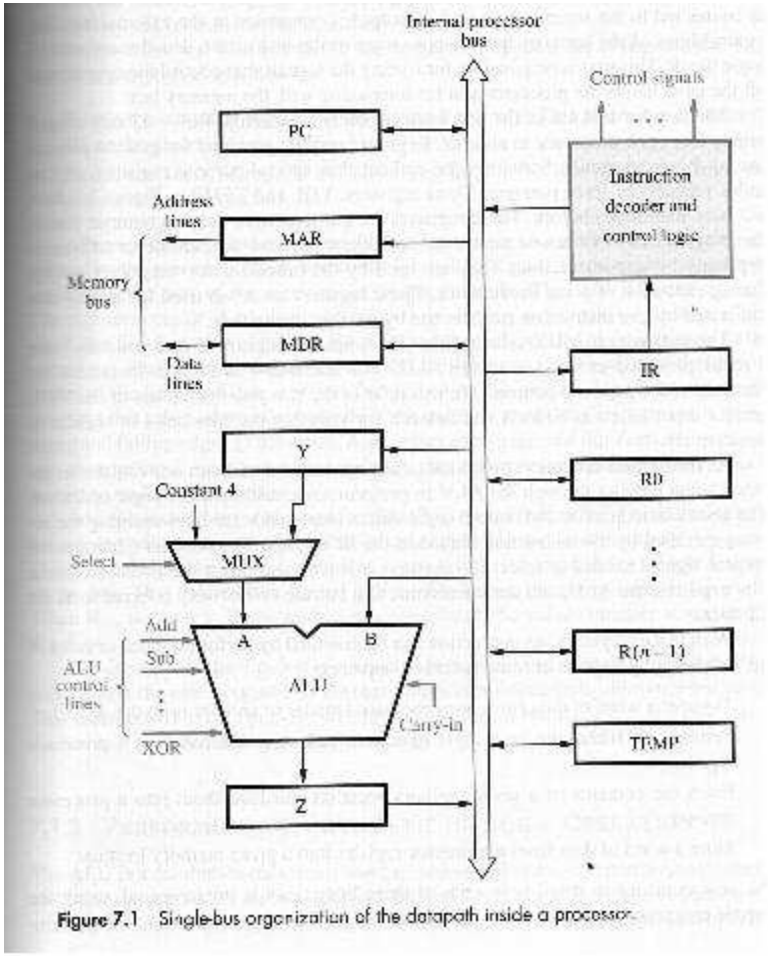

Figure 7.1 Single-bus organization of the datapath inside a processor.

Isochronous Timing

- Devices that operate independently of the CPU clock BUT
- The application requires a constant time of operation between successive occurrences.
- Keyboard, mouse are asynchronous as they can occur at any time and independent of the CPU timing
- Speech samples are isochronous as they have to happen at a precise time- ie the sampler must be precise at the A/D converter.
- The output digital samples to the analogue converter must also be sent at precise times for the speech (music) to be natural

Universal Serial Bus

- A simple, low cost,interconnection system
- Accommodate a wide range of I/O devices and bit rates, including Internet connections, and audio and video applications
- Enhance user convenience through the ‘plug and play’ mode of operation
- Each device on the USB is assigned a 7-bit address, local to the USB tree, not related to the processor’s address space.

Three Internal Buses in a CISC Processor

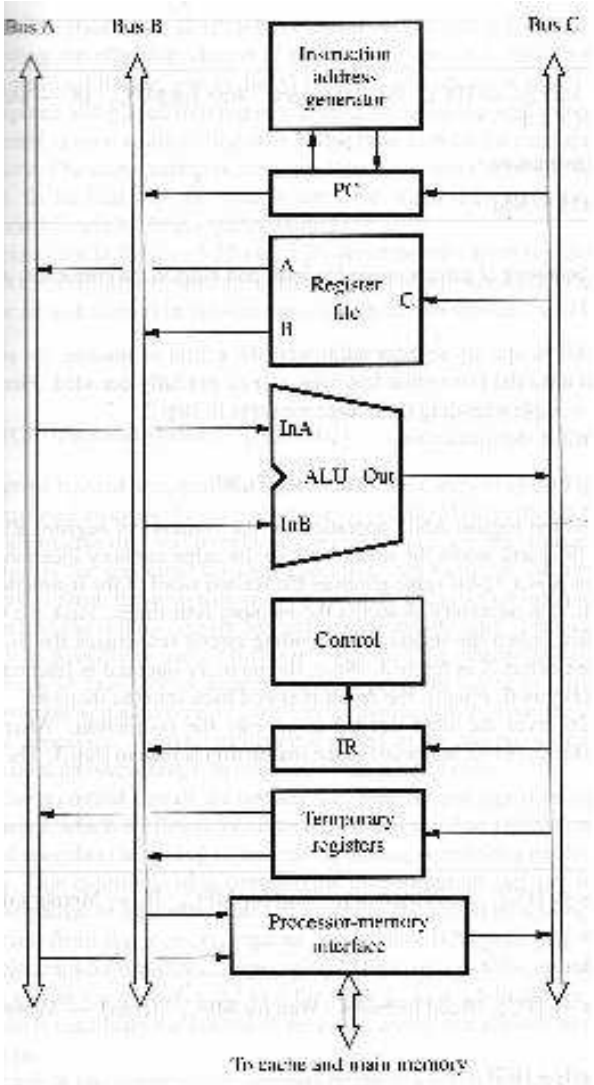

Figure 5.24 Three-bus CISC-style processor organization.