Department of Communications and Computer Engineering
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CCE 1011 Introduction to Computer Systems

Tutorial Cache Memory

1. A computer system has a main memory consisting of 1M 16-bit words. It has also a 4K-word cache organized in a block-set-associative manner, with 4 blocks per set and 64 words per block.

(a) Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. *(12,2,6)*

(b) Assume that the cache is initially empty. Suppose that the processor fetches 4352 words from locations 0 , 1, …to 4351 in that order. It then repeats this fetch sequence nine more times.

If the cache is ten times faster than main memory, estimate the improvement factor resulting from the use of the cache. Assume that the Least Recently Used (LRU) algorithm is used for block replacement.

(taken from Hamacher, Vranesic &Zaky, 5.10)

(2.33)

2. Repeat 1 using the MRU algorithm

(4.21)

3. A system has a small cache of eight 32-bit words and a main memory of 1KB (256 words). Data are transferred to cache 4 consecutive bytes at a time on a proper word boundary. The following sequence of main memory addresses (in hexadecimal) are required by the CPU

54, 58, 104, 5C, 108, 60, F0, 64, 54, 58, 10C, 5C, 110, 60, F0, 64.

Initially the cache is empty. Determine whether each address produces a hit or a miss for

(i) direct mapping . Initially work out the number of bits in the TAG, BLOCK and WORD fields *(5,3,2) (5 hits, 11 misses)*

(ii) two-way set associative using the LRU algorithm. Initially work out the number of bits in the TAG, SET and WORD fields.
(5,2,2) (3 hits, 15 misses)

(taken from Mano&Kline,14.1)

4. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. A program executes using the following sequence of hex addresses

200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4

This pattern is repeated four times.

(i) Show the contents of the cache at the end of each pass through the loop if a direct mapped cache is used. Compute the hit rate. Assume the cache is initially empty.

(Pass1 H 3, M 9; Pass2-4 H10, M2)

(ii) Repeat part (i) for an associative mapped cache that uses the LRU replacement algorithm. *(Pass1-4 H3, M 9)*

(iii) Repeat (i) for a four-way set-associative cache.

(Pass 1 H3 M 9; Pass 2-4 H7 M 5)

(taken from Hamacher, Vranesic &Zaky, 5.13)

5. A computer has a 32-bit address and a direct mapped cache. Addressing is to the byte level. The cache has a capacity of 1 K bytes and uses lines of 32 bytes.?

(i) Work out the number of bits in the TAG, INDEX(BLOCK) and LINE (WORD) fields of a main memory address.

(22, 5, 5)

6. A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.

(a) How many bits are there in main memory address? *(19)*

(b) How many bits are there in each of the TAG, SET and WORD fields?

(taken from Hamacher, Vranesic &Zaky, 5.9)

(8,4,7)