Department of Communication and Computer Engineering
Faculty of ICT
CE1011 Introduction to Computer Systems
CCE1012 Computer Logic and Organisation

Tutorial_RAM

1. Distinguish between static RAM and dynamic RAM. Why is a refresh circuit necessary in a dynamic RAM system?

2. Is cache memory made up of static or dynamic RAM? Give reasons

3. If a processor has a 28 bit address line, what is the maximum range of memory addresses it can have?

4. Draw a block diagram of a RAM, organised as a 1024 X 1 bit, that uses RAS and CAS control.

5. Draw a block diagram of a byte (8 bit)organised memory making use of an 1024X1 bit memories. Indicate clearly the address bus connections.

6. A 1 Gb RAM has effectively approximately 1.25 Gb memory cells. Give reasons why this is so.

7. Consider a dynamic RAM that must be given a refresh cycle 64 times per millisecond. Each refresh operation requires 150 ns. A memory cycle requires 250ns. What percentage of the memory's total operating time must be given to refreshes*? Ans 0.96%*

8. Design an 8-bit memory of total capacity 2048 addresses using SRAM chips of 1024X1 bits. Indicate clearly the organisation of the address bus and of the memorry data buffer wrt to the memory system.

9.A main memory RAM made up of eight bits per address b_7 to b_0. It has two extra check bits added defined as $b_8 = b_0 \oplus b_3 \oplus b_6 \oplus b_7$; $b_9 = b_0 \oplus b_1 \oplus b_5$;

Work out the check bits associated with:
10001100 00011111 *Ans 00, 00 (in both cases)*
Note that b_0 is the rightmost (least significant) bit.

Is the data 1010101010 a correct memory word? Give reasons
No should be 0010101010

10. What is the main use of read only memory in a computer system motherboard?