CCE1012          Computer Logic and Organisation
Answer ANY FOUR questions


1.  Write short notes on the following:
        (a) synchronous and asynchronous clock
        (b) overflow detection in the ALU
        (c) optical disk storage
        (d) write policy when using cache memory
        (e) instruction fetch in today's CPU's

                                                    (25 marks)


2. a) Four benchmark programs are executed on three computers. In each case the
execution time, in seconds, was measured. Each program had 100,000,000
instructions. Table 1 gives the time, in seconds, that each computer took to execute
each program.                                              (10 marks)


|            | Computer A | Computer B | Computer C |
|------------|------------|------------|------------|
| Program 1  | 1          | 10         | 20         |
| Program 2  | 100        | 100        | 20         |
| Program 3  | 500        | 1000       | 50         |
| Program 4  | 100        | 800        | 100        |

Table 1

Calculate the average MIPS for each computer using the suite of four programs.

    b)      A  256 X 1 bit RAM IC is to be used in building a 1024 X 8 memory bank

        (i)     How many IC's are necessary?            (3 marks)

        (ii)    Sketch the memory making use appropriately of a suitable decoder,
                chip enables and IC banks. Describe briefly your sketch.

                                                        (8 marks)
        (iii)   For your sketch show via the decoder which bank is used to access
                the data from address 345.              (4 marks)


3.      A small computer has a main memory with 16 address bits. Addressing is to
        the byte level.
        The cache has a capacity of 2K bytes. The block transfer between memory and
        cache is of 64 bytes. The cache uses a set associative organisation using 2
        blocks per set.
                (i)     How many bits are there in the TAG, SET and WORD fields.
                                                        (6 marks)
                (ii)    The following main memory blocks are to be transferred to
                        cache. In each case the start address of the block, in
                        hexadecimal, is given.
                            AF80, AC80, CF00, CFC0.

For each address work out the value of the tag and the set fields, in decimal.

(16 marks)

(iii)     Do the four main memory blocks map to different sets? Give reasons for your answer.

(3 marks)

4.   (a) Minimise the following four bit logic system using Karnaugh map techniques.

$$F(A,B,C,D) = \Sigma m_0, m_2, m_4, m_5, m_8, m_{10}, m_{12}$$

(10 marks)

(b)  An ALU has a parallel full adder. Given the inputs to one full adder stage, $A_i$, $B_i$, and $C_i$, give the truth table and hence the function, for the sum $S_i$, and the carry $C_{i+1}$.          (6 marks)

(c) What is the valid range for an 8-bit two's complement number representation?          (4  marks)

(d) Give the truth table for a 2 to 4 binary decoder, and hence draw the decoder using logic gates.          (5 marks)

5.   (a) An 8-bit register contains the binary pattern A3 in hexadecimal. Starting with this pattern in both cases, work out the contents of the register, in hexadecimal, after:
   (i)      an arithmetic shifts right;
   (ii)     a rotate left by one bit

(8 marks)

(b) Using Booth's algorithm and a 5-bit two's complement representation work out the following multiplication:
          Multiplicand  -15;   Multiplier   13

(9 marks)

(c)     A hard disk drive volume has 12 surfaces and has 10,000 tracks. Each track has 400 sectors, with 512 bytes per sector.
   (i)      Calculate the volume data capacity in Megabytes.

(3 marks)

   (ii)     Suggest a suitable address format for the disk volume.

(5 marks)