A Dummy- Paper for Computer Architecture CCE3013

This is typical of how questions will be set. The actual material covered within any of these questions can be altered in the exam paper. The material examinable is what has been covered in the class and not restricted solely to what is covered in these questions.

Answer any FOUR questions.

1. (a)Describe three ways in which a conditional branch instruction can be handled in a pipeline. (8 marks)

(b) A processor has a four stage pipeline. The processor also uses an instruction cache and a data cache. The system clock operates at 500MHz, and each pipeline stage requires two clocks for proper operation. An external memory read/write requires 30ns. A programme has 10% of the instructions requiring external memory access. 20% of instructions require data operands, and 10% of these operands need to be accessed from main memory.

(i) Calculate the average number of clock cycles that are necessary to allow for the pipeline stalls, and the resultant speed up compared to sequential execution. (5 marks)

(ii) Additionally pipeline stalls due to data dependency increase the execution penalty by 0.5 clock cycles. (6 marks)

(iii) To keep the resultant speed up factor the same as in (i) it is necessary to reduce the percentage of data operands that are required from main memory. Calculate this new percentage value. (6 marks)

2 (a) (i) Mention and define four types of computer architectures that allow parallelism for instruction execution and data execution.

: (ii) Which one of the four types you defined above is the LEAST ONE used in practice. Give reasons for your answer. (6 marks)

(b) (I) Define the terms (i) arc connectivity
(ii) number of links
for a computer communication network. (4 marks)

(II) What are the values of arc connectivity and number of links for
(i) a 3-D hypercube; (ii) a 2-D ring with 16 nodes (3 marks)

(c) A computer system has to add 150,000 numbers. The multiprocessor architecture available is a binary tree architecture with 15 processors;

The data is initially in the root processor . The data is to be shared equally between all processors, and must first be passed to each processor before the addition starts. The partial answers must be accumulated and passed back to the original start processor.

The overheads per processor interconnect transfer are:
(i)every 2000 data transfers equivalent to 1 addition unit;
(ii)a fixed overhead equivalent to 100 addition units.
Every interconnect can be used simultaneously with one transfer message. Estimate the processing time in number of addition units. State any assumptions made. (12 marks)

3 (a) Use Booths recoding algorithm show how to obtain the two's complement 8-bit multiplication of -25 Multiplicand
44 Multiplier (8 marks)

(b) For the principle collision vector

1 0 0 0 1 1

Draw the reduced state-diagram (9 marks)
and hence show

(i) the greedy cycle

(ii) the maximum-rate cycle using the following collision vector. (8 marks)

4. (a) What is the meaning of superscalar execution? (5 marks)

(b) One of the methods that are used in pipelining is dynamic branch prediction. Design a simple algorithm that can be used for dynamic branch prediction. Explain clearly its operation. (8 marks)

(c) What is the meaning of 'a thread' in parallel processing? (6 marks)

(d) What is a barrel shifter. Illustrate a procedure that can be used to achieve a shift operation in a barrel mode. (6 marks)

5. A processor pipeline with four stages - Fetch,Decode,Execute,Writeback, has the following sequence of instructions:

```
        ADD   R0,R1,R2
        MUL   R3,R2,R4
        MOV   #05, R0
LAB1:   INC   R4
        DEC   R0
        JNZ   LAB1
```

Initially R0 =20, R1 = 10, R2=05, R3=25

(i) Using the pipeline show where there are:
Data dependencies and branch delays (4 marks)

(ii) Assuming each pipeline stage executes in one time unit, what is the overall speed up compared to direct sequential execution, taking into account any pipeline stall that is necessary for correct operation. (4 marks)

(iii) Suggest alterations in the instruction sequence that can improve the efficiency of the pipeline, and work out the new speedup factor. (4 marks)

(b) A system is to pass data from source to destination via four nodes. The data to be transferred is 120,000 bits. When broken down into packets, each packet requires 256 bits as additional control bits independent of the packet size. Cut-through routing is available, and the system speed is 1 Mbps. Any packet requires 10 ms of service time from the time it is received to the time when it starts to transfer, (or in the last node to be abutted properly in the original data). Calculate the time taken if

(i) packets of 20,000 data bits are used

(ii) packets of 2000 data bits are used.

Comment on your results. (13 marks)