Computer Logic and Organisation CCE1012 June 2010
Answer ANY FOUR questions. All questions carry equal marks.

1. Write short notes on the following:
(i) overflow detection in integer arithmetic
(ii) magnetic disk access time
(iii) static and dynamic RAM
(iv) write policies in cache memory
(v) error correcting codes in RAM
(25 marks)
2. (a) A processor operates at a clock of 1 GHz . It has four basic types of instructions with the following execution time in terms of clock cycles:

| Transfer instruction | 3 clocks |
| :--- | :--- |
| ALU integer | 2 clocks |
| ALU floating point | 5 clocks |
| Decision instruction | 6 clocks |

(i) Calculate the time, in nanoseconds, for the execution of one instruction of each type.
(b)A program using the processor in (a) above has the following instruction mix:

Transfer instructions 20,000
ALU Integer instructions $\quad 40,000$
ALU floating point instructions $\quad 30,000$
Decision instructions 10,000
(i) Calculate the time to execute the program, and
(10 marks)
(ii) the resulting average MIPS for this program.
(7 marks)
3 (a)A computer system has a main memory of 64 kilobytes. It uses a small cache memory of 2 kilobytes organised into 8 sets with 2 blocks per set.
(i)Calculate the TAG, SET and WORD fields of a main memory address.
(6 marks)
(b) The following main memory blocks are to be transferred to cache. In each case the start address of the block, in hexadecimal, is given.

8F80, 6C80, CF00, AFC0.
(i)For each address work out the value of the tag and the set fields, in decimal.
(16 marks)
(ii)Do the four main memory blocks map to different sets? Give reasons for your answer.
(3 marks)
4. (a) A 256 X 1 bit RAM IC is to be used in building a $512 \times 16$ memory bank(ie a memory bank with 512 memory addresses and 16 bits per address)
(i) How many IC's are necessary? (3 marks)
(ii) Sketch the memory making use appropriately of a suitable decoder, chip enables and IC banks. Describe briefly your sketch.
(5 marks)
(iii) For your sketch show via the decoder which bank is used to access the data from address 145 .
(4 marks)
(b) A magnetic disk has a diameter of 10 cm . Tracks are manufactured on the platter starting at $\mathrm{r}=2.5 \mathrm{~cm}$ to $\mathrm{r}=4.5 \mathrm{~cm}$. Each track is spaced by 0.1 mm . The data is organised in 200 sectors per circumference, each sector containing 1024 bytes of data.
Calculate
(i) the number of tracks (4 marks)
(ii) the maximum and minimum bit density in, bits per mm, along a track.
(6 marks)
(iii) If the platter rotates at a speed of 2400 revolutions per minute, calculate the average rotational delay. (3 marks)
5. (a) Minimise the following four bit logic system using Karnaugh map techniques.

$$
\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\Sigma\left(\mathrm{m}_{0}, \mathrm{~m}_{1}, \mathrm{~m}_{3}, \mathrm{~m}_{7}, \mathrm{~m}_{8}, \mathrm{~m}_{9}, \mathrm{~m}_{11}, \mathrm{~m}_{15}\right)
$$

(6 marks)
(b) Give the truth table, and hence the logic function, of one bit full adder whose inputs are $A_{i}, B_{i}$, and $C_{i}$ and the outputs are $S_{i}$ and $C_{i+1}$
(5 marks)
(c) For a 5-bit fast adder IC
(i) how many pins are necessary on the IC. Give reasons
(3 marks)
(ii) the internal carry of the fast adder is based on the relation
$\mathrm{C}_{\mathrm{i}+1}=\mathrm{C}_{\mathrm{i}} \mathrm{P}_{\mathrm{i}}+\mathrm{G}_{\mathrm{i}}$
What is $\mathrm{P}_{\mathrm{i}}$ and $\mathrm{G}_{\mathrm{i}}$ in terms of the 2 corresponding number bits, $\mathrm{A}_{\mathrm{i}}$ and $\mathrm{B}_{\mathrm{i}}$, to be added?
(2 marks)
(iii) Work out the relationship for the output carry, $\mathrm{C}_{5}$, from the IC in terms of the P's and the G's (5 marks)
(d) An 8-bit register contains the binary pattern 73 in hexadecimal.

Starting with this pattern in both cases, work out the contents of the register, in hexadecimal, after:
(i) an arithmetic shift left;
(ii) a rotate right by one bit

