1. Define the basic performance equation. Find the processor time required to execute 500 instructions on a 166MHz processor, assuming that on average one instruction requires 3 steps.

2. Explain pipelining and superscalar operation.

3. Describe the space-time diagram and give a practical example for a 6-stage pipeline.

4. Define the ideal speedup of a pipeline circuit.

5. What is the speedup of an 8-stage ideal pipeline producing (a) 10 items, (b) 200 items, (c) 3000 items, and (d) 600,000 items.

6. Define the practical speedup of a pipeline and indicate the causes of the loss in speedup with respect to the ideal case.

7. What is the speedup of a 9-stage pipeline having a total buffer delay of 50 ns and processor speed of 1 MHz when executing (a) 50 items, (b) 160 items, and (c) 4500 items. State any assumptions made.

8. Define the efficiency of a pipeline and find the efficiency of an ideal 5-stage pipeline operating on (a) 10 data elements, (b) 200 data elements, and (c) 1200 data elements.

9. Explain the requirement of a cache memory in pipelined systems.

10. Indicate reasons that will cause a pipeline to stall.

11. Explain data hazards, indicating how their effect can be reduced in hardware and in software.

12. Describe side effects in data hazards.

13. Explain instruction hazards indicating methods used to reduce their effect on performance.

14. Explain how addressing modes and conditional codes affect the performance of the pipeline.

15. The figure below shows a 4-stage pipeline architecture. Assuming each stage requires on clock cycle to execute, give the contents of the buffer registers over the first 12 cycles for the following instruction set:
ADD  R1, R2, R3 ;add R1 to R2 storing in R3
SUB  R5, R4, R1 ;subtract R4 from R5 storing in R1
LD   R2, ADDR1 ;load into R2 from memory ADDR1
ST   R3, ADDR2 ;store contents of R3 in memory ADDR2
ADD  R4, R1, R1 ;add R4 to R1 storing in R1
ST   R1, ADDR3 ;store contents of R1 into memory ADDR3

Assume the contents of the registers and ADDR1 are:
R1 = 25, R2 = 38, R3 = 45, R4 = 60, R5 = 15, and ADDR1 = 80.

16. Calculate the performance gain of a 5-stage pipeline having a rate of 600 MHz. Assume that 25% of the instruction access data in memory, having 92% instruction hit rate and 86% data hit rate. Assume that the access to main memory takes 14 clock cycles.

17. If a secondary cache were placed between the processor’s cache and main memory having average access time of 8 clock cycles, what would be the gain in performance in (16)? Take the secondary cache hit rate to be 93%.

18. Compare the CISC and RISC architectures.

19. Describe the operation of a barrel shifter.

20. Sketch the logic gate design for bit 0 of a 16-bit shift right register using barrel shifting techniques. Illustrate clearly how bit 0 becomes bit 9, including the necessary control logic to achieve this shift.